

PRIOR ART

FIGURE 1

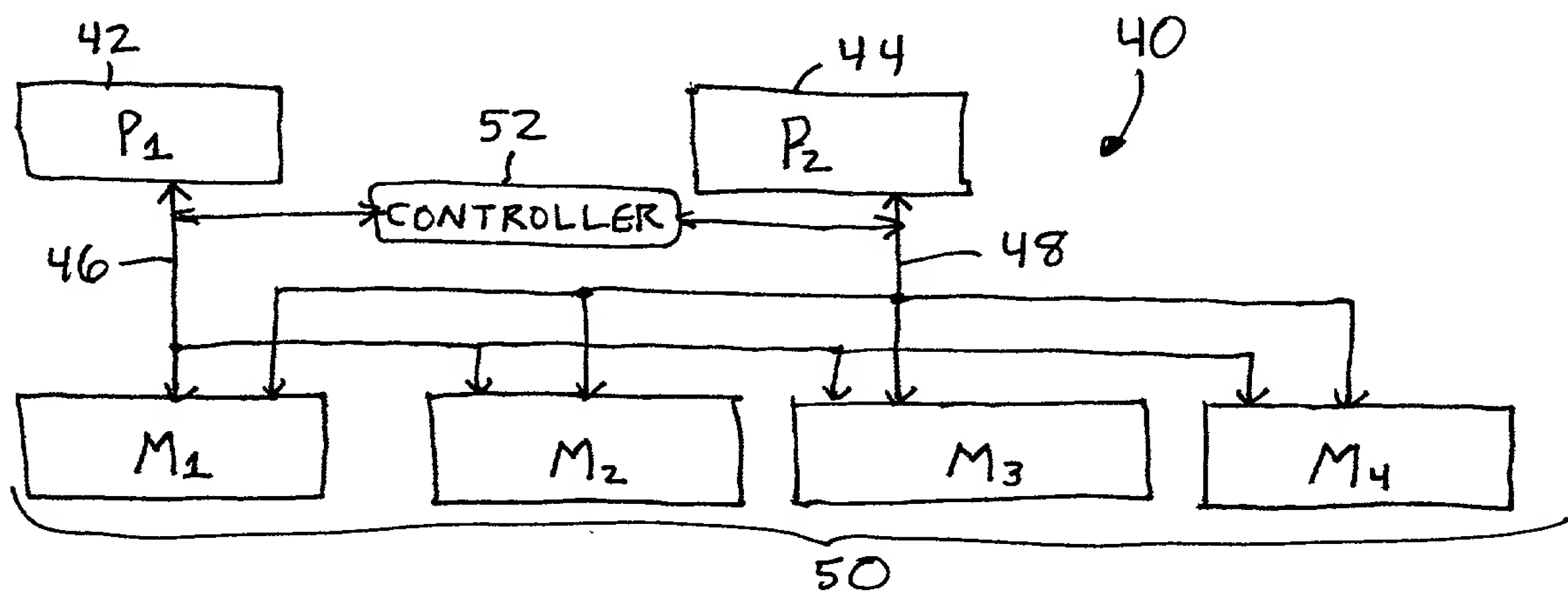


FIGURE 2

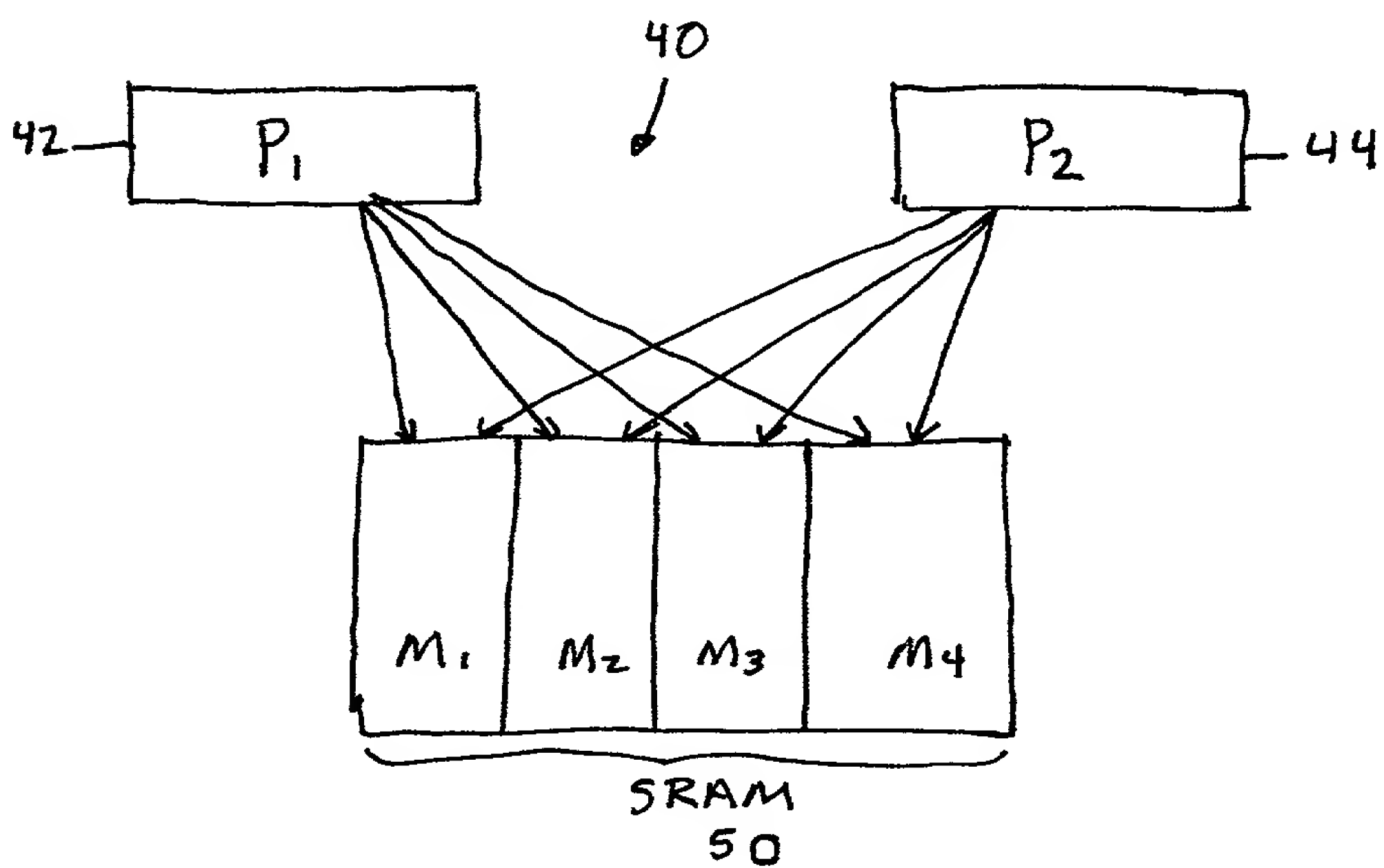


FIGURE 3

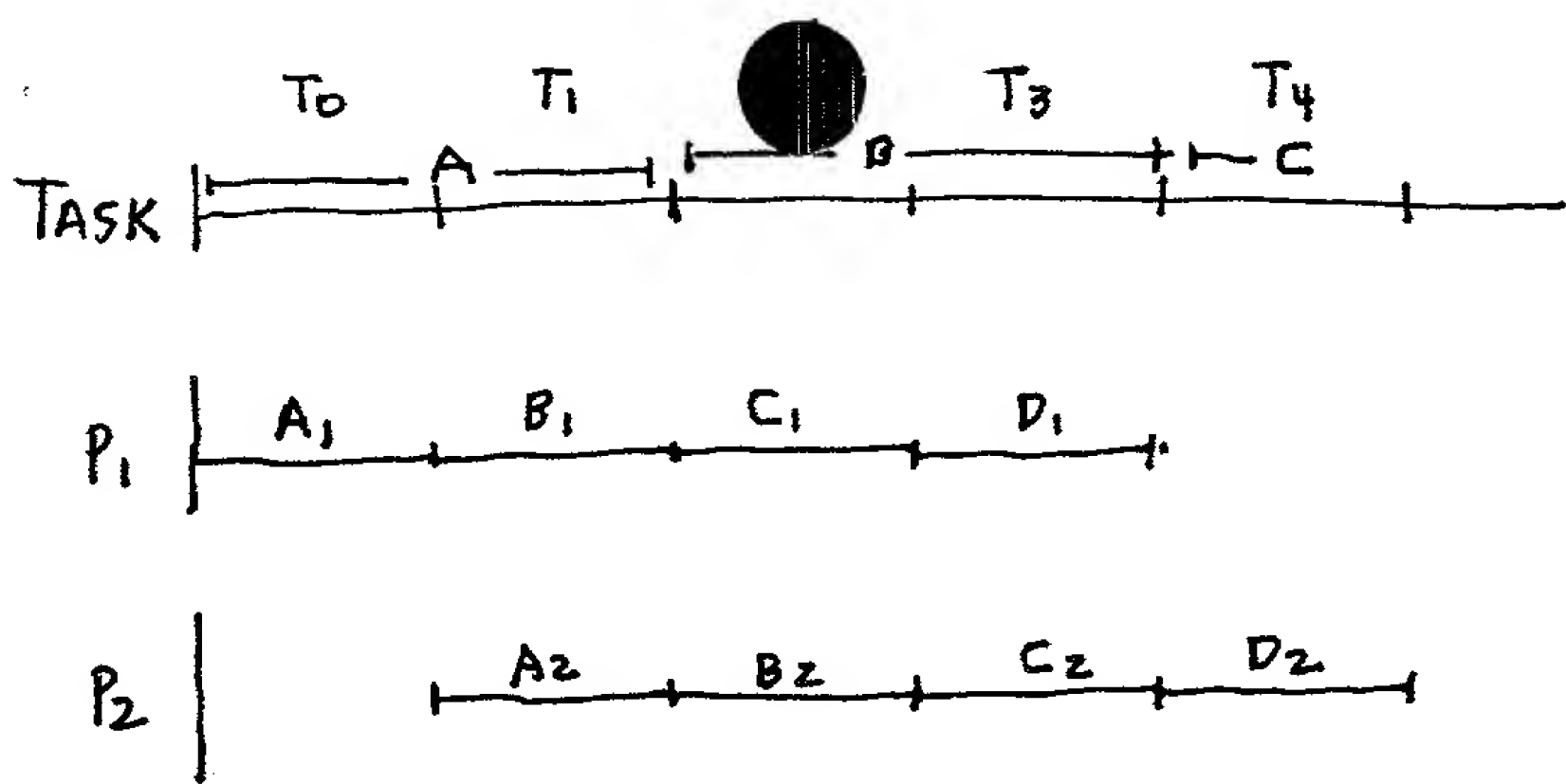


FIGURE 4

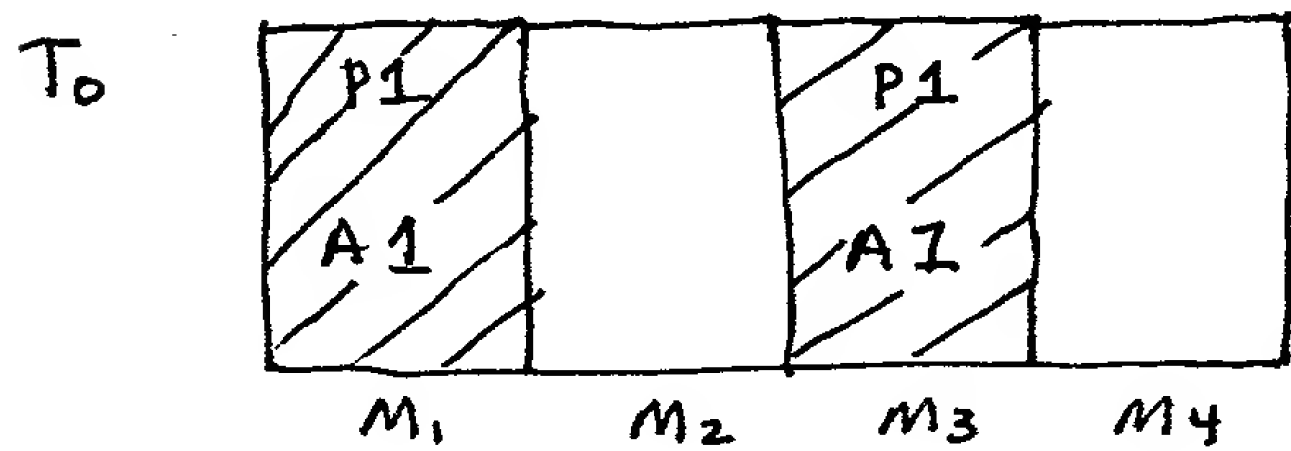


Figure 5A

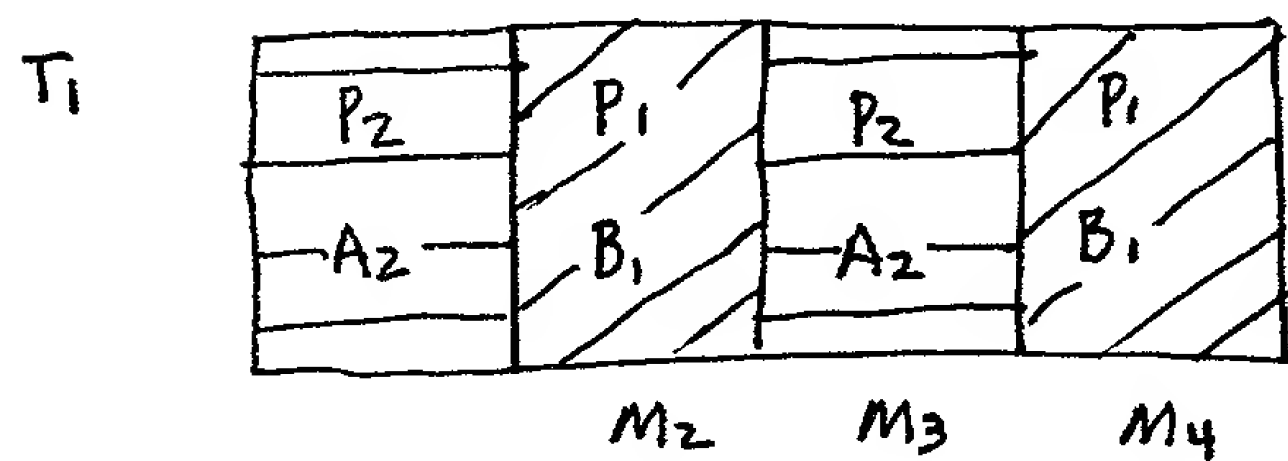


Figure 5B

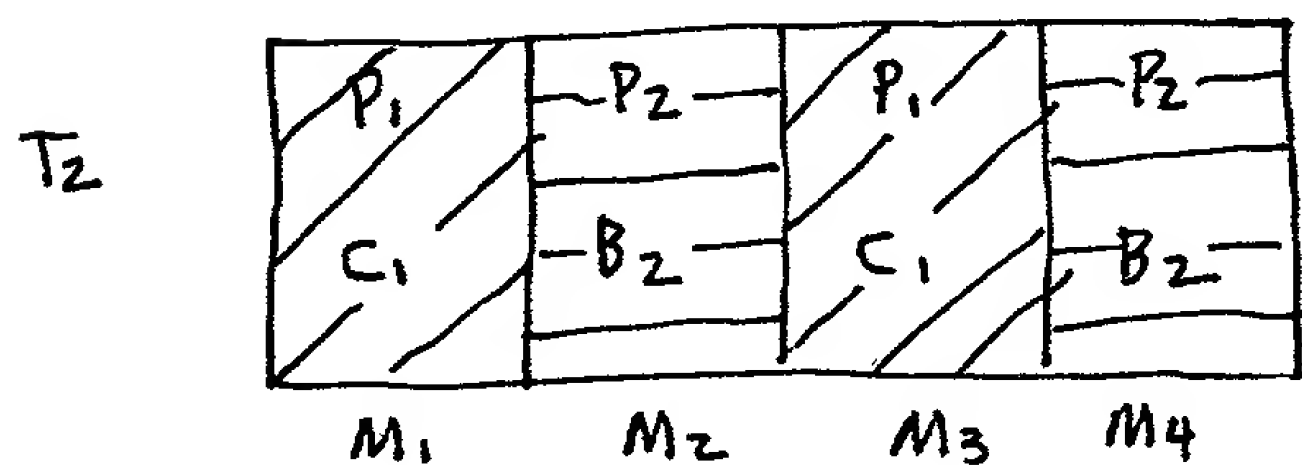


Figure 5C

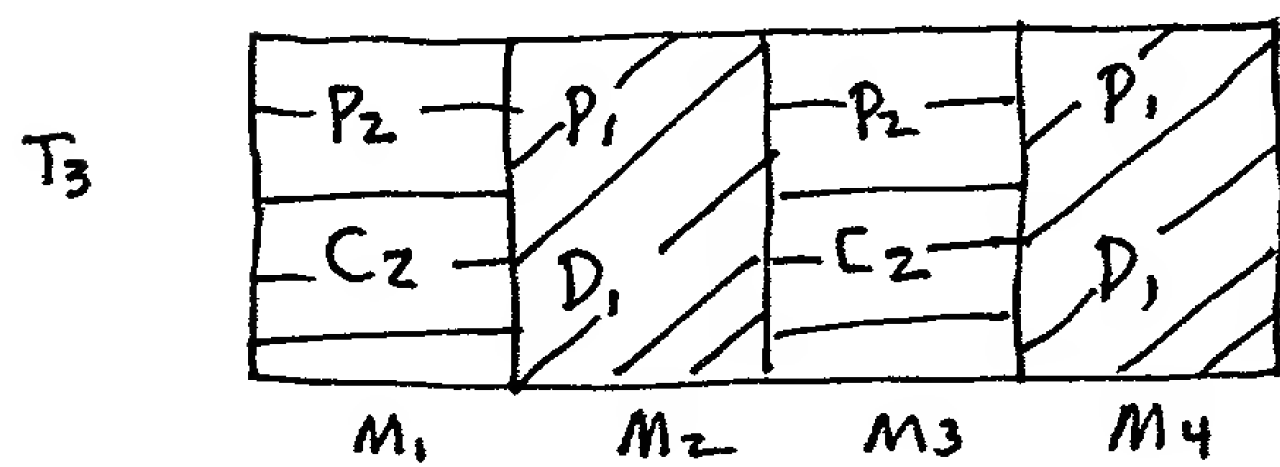


Figure 5D

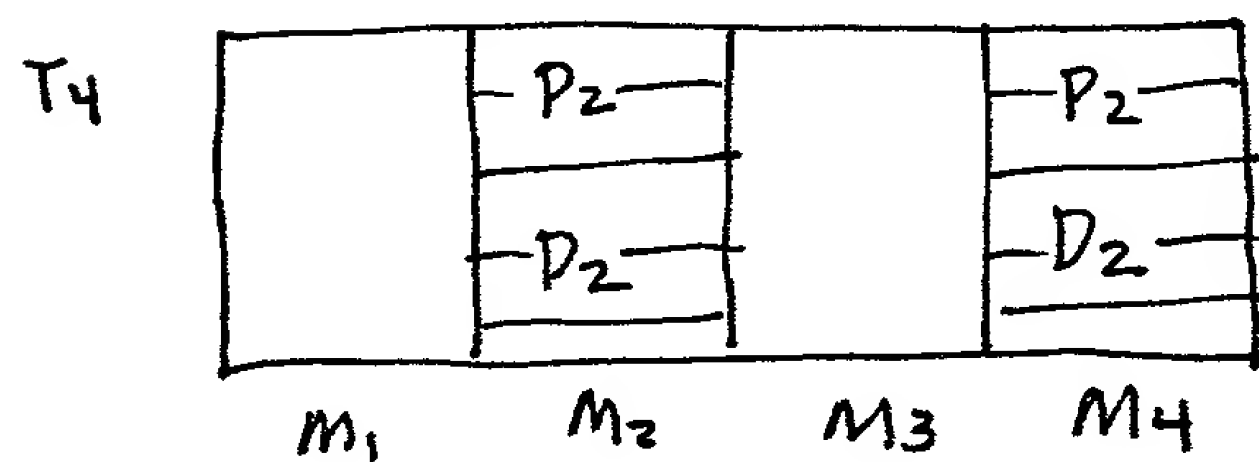


Figure 5E



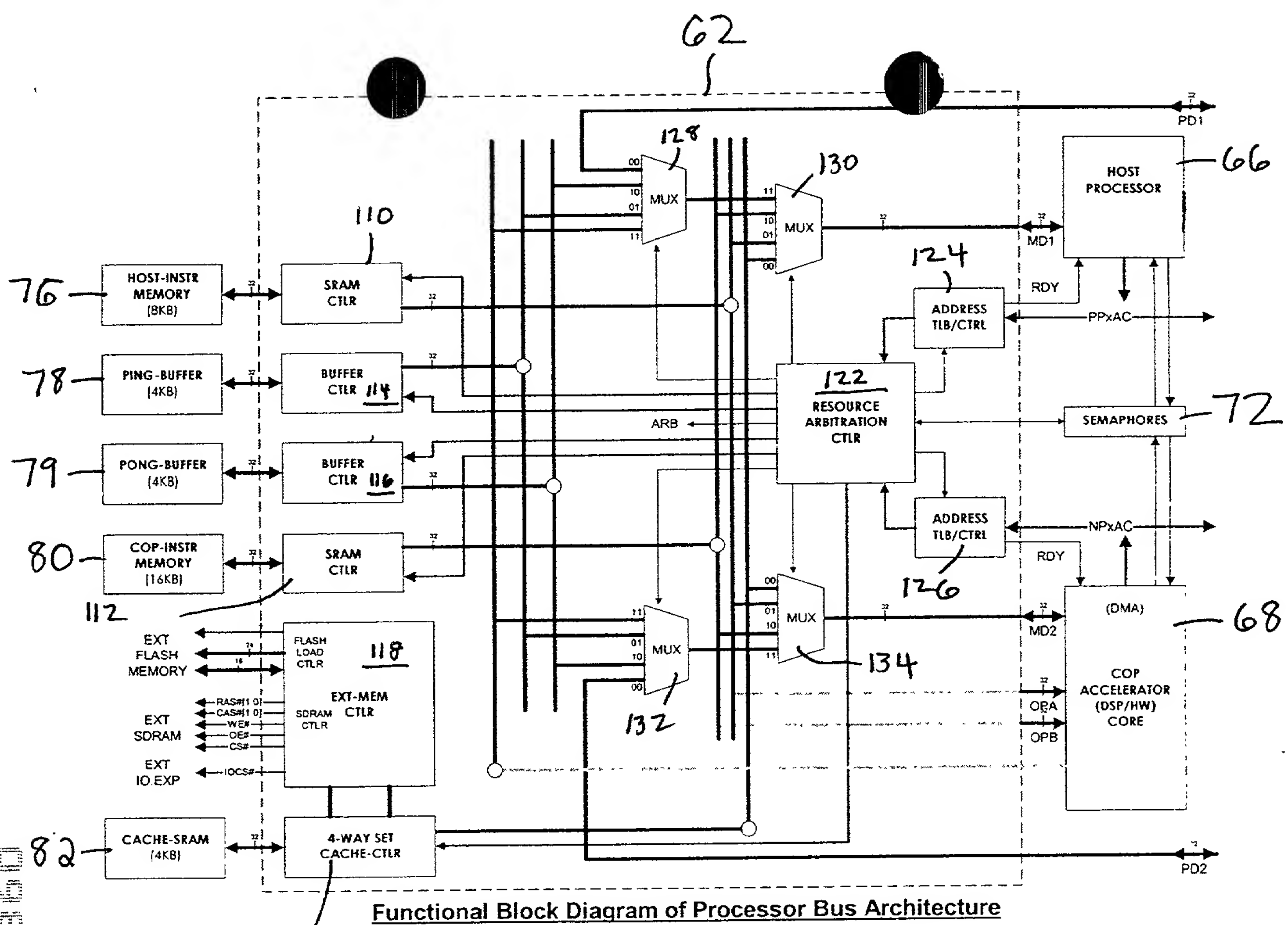


Figure 7

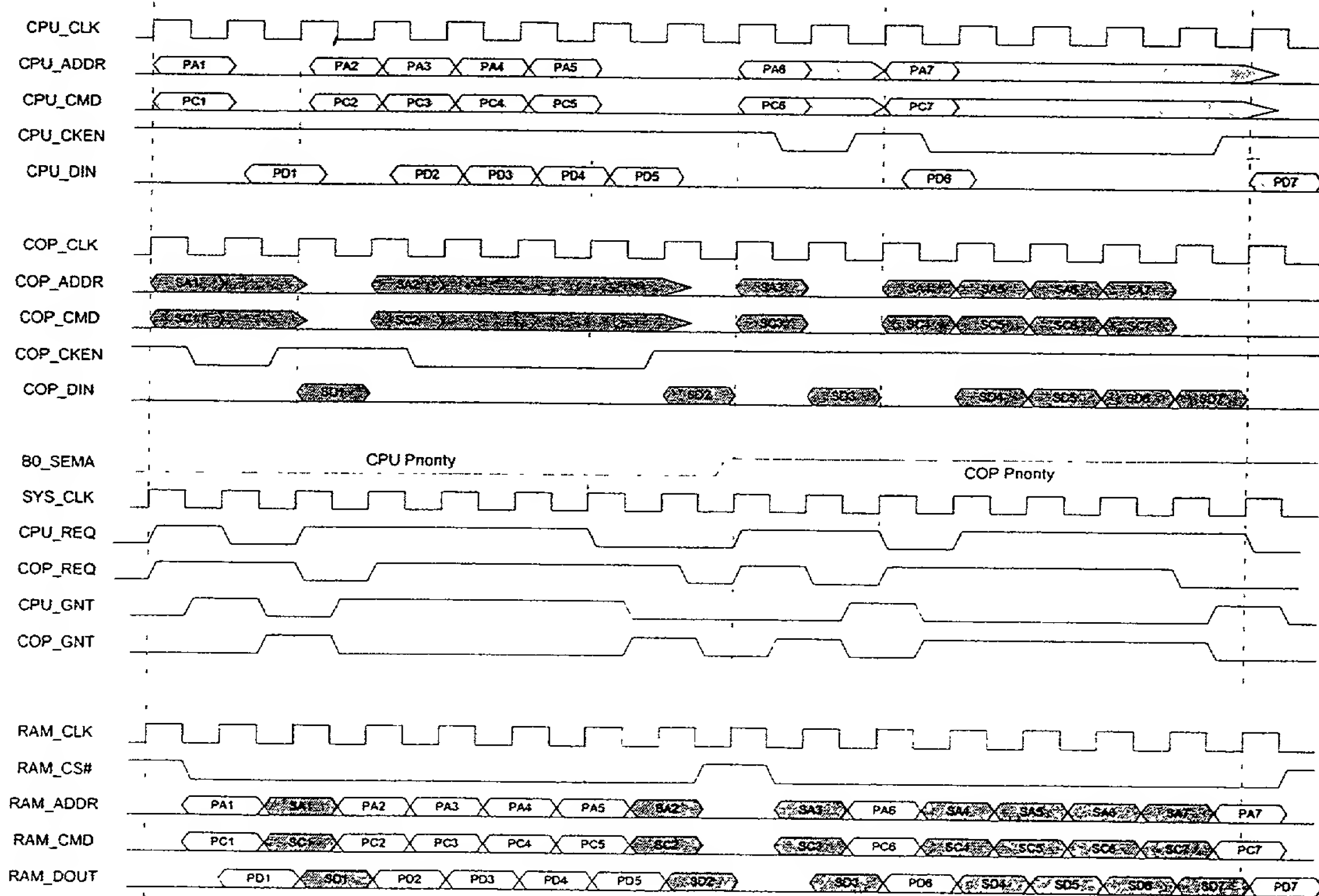
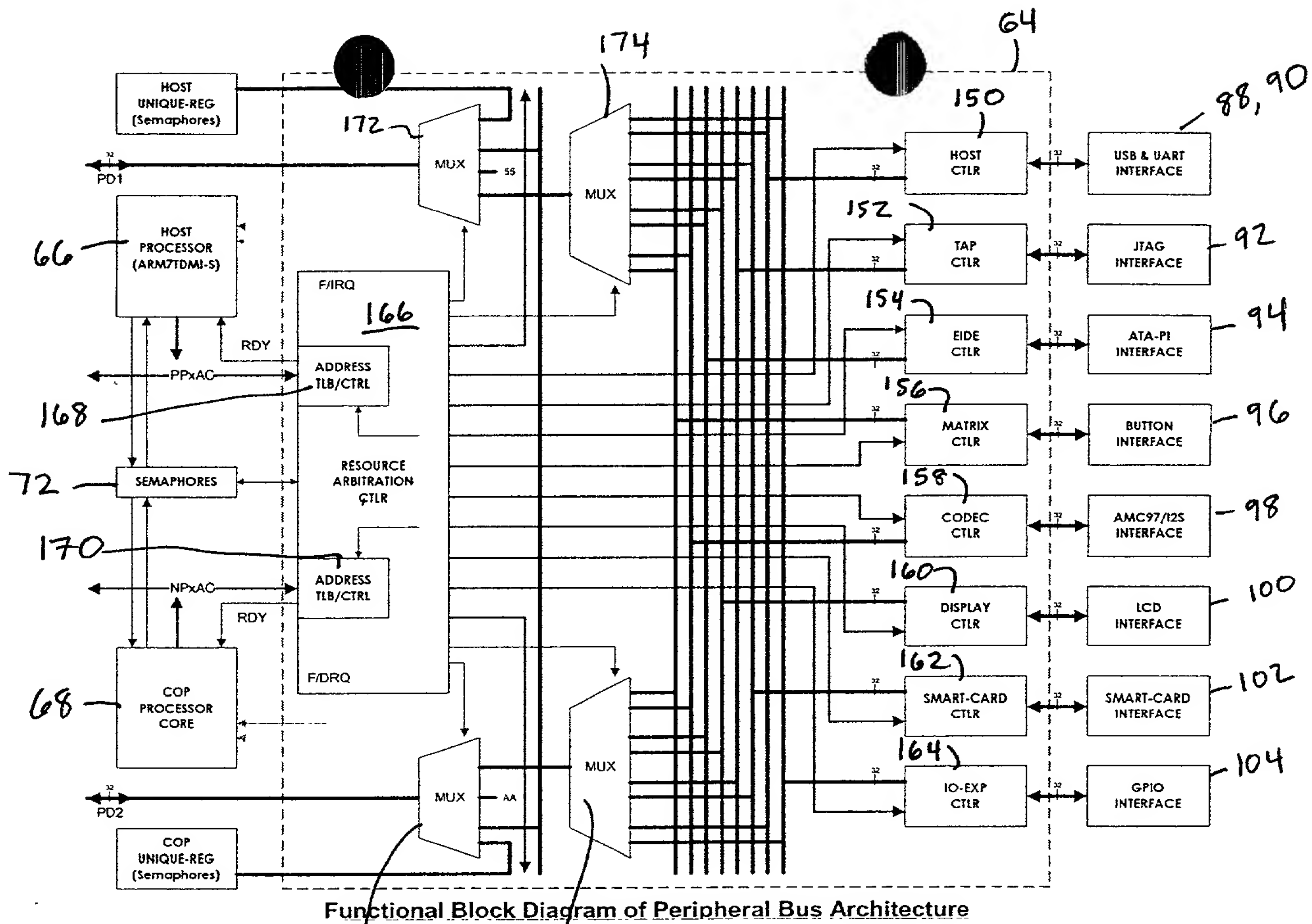


Figure 8



Functional Block Diagram of Peripheral Bus Architecture

Figure 9

